Lesson 8: Analog Signal Conversion

ET 438b Sequential Control and Data Acquisition

Department of Technology

Learning Objectives

After this presentation you will be able to:

- Determine the resolution and accuracy of a digitized analog signal.
- Explain how digital-to-analog converts operate
- Explain how commonly used analog-to-digital converts operate
- Compare and contrast the characteristics several commonly used analog-to-digital converters.

Analog Signal Conversion

Two Problems

Input — Analog-to-digital conversion (ADC): continuous signals converted to discrete values after sampling

Output — Digital-to-analog conversion (DAC) Discrete values converted t continuous signals

Number of bits in digital signal determines the resolution of the digital signals. Resolution also depends on voltage

Resolution and Accuracy of Digitized Signals

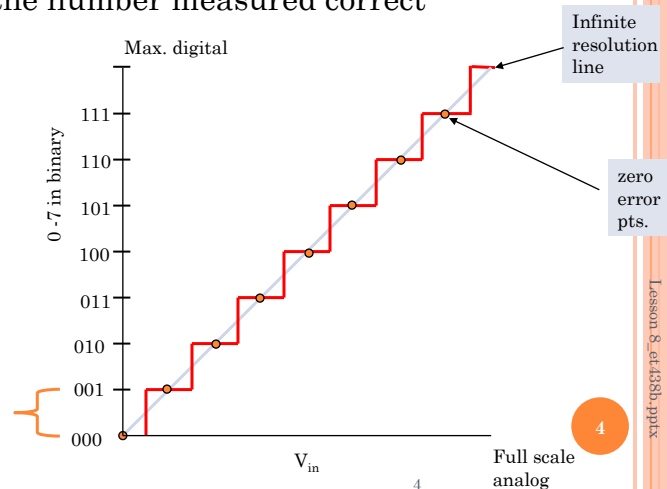
Resolution - smallest number that can be measured

Accuracy - is the number measured correct

ADC Resolution

The output is a discretized version of the continuous input.

Error determined by the step size of the digital representation



Resolution Formulas

Resolution, in terms of full scale voltage of ADC, is equal to value of Least Significant Bit (LSB)

$$V_{LSB} = \frac{V_{fs}}{2^n}$$

Where V_{fs} = full scale voltage
n = number of bits
V_{LSB} = voltage value of LSB

Finite bit digital conversion introduces quantization errors that range from $\pm V_{LSB}/2$

Maximum quantization error is $Q.E. = \frac{V_{LSB}}{2}$

Where Q.E. = quantization error
V_{LSB} = voltage value of LSB

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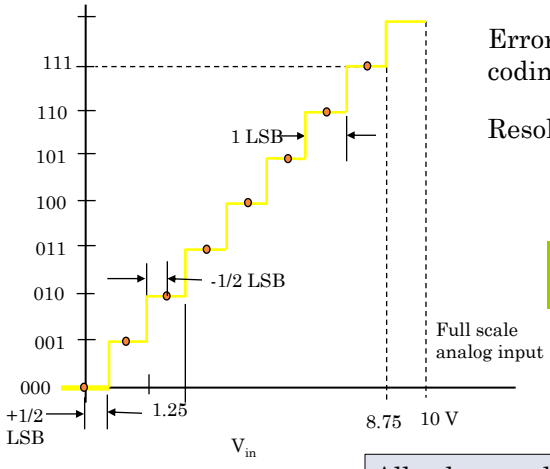
Digital Resolution and Error in ADC



Error in natural binary coding is ±1/2 LSB

Resolution 3-bit system

$$V_{LSB} = \frac{V_{fs}}{2^n}$$

$$V_{LSB} = \frac{10V}{2^3} = \frac{10}{8} = 125$$

All voltage values between 8.75-10 V map to the 111 code
Number of counts reduced by 1

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RESOLUTION FORMULAS

Percent Resolution- Based on the number of transitions (2^{n-1})

$$\%\text{resolution} = \frac{1}{2^n - 1} \cdot 100\%$$

Where n = number of bits in digital representation

Example 1: An 8-bit digital system is used to convert an analog signal to digital signal for a data acquisition system. The voltage range for the conversion is 0-10 V. Find the resolution of the system and the value of the least significant bit

n=8 so signal converted to 256 different levels.
V_{fs}=10 Vdc

$$V_{LSB} = \frac{V_{fs}}{2^n}$$

$$V_{LSB} = \frac{V_{fs}}{2^n} = \frac{10\text{ V}}{2^8} = \frac{10}{256} = 0.0390625\text{ V}$$

$$\%\text{resolution} = \frac{1}{2^n - 1} \cdot 100\%$$

$$\%\text{resolution} = \frac{1}{2^8 - 1} \cdot 100\%$$

$$\%\text{resolution} = 0.392\%$$

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Example 2: The 8-bit converter of the previous example is replaced with a 12 bit system. Compute the resolution and the value of the least significant bit.

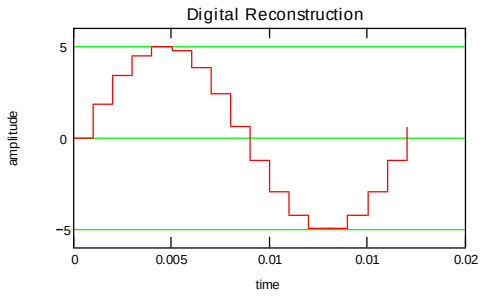
Signal converted to 4096 different levels n = 12

$$V_{LSB} = \frac{V_{fs}}{2^n}$$ n = 12 bits V_{fs} = 10 Vdc $$V_{LSB} = \frac{V_{fs}}{2^n} = \frac{10\text{ V}}{2^{12}} = \frac{10}{4096} = 0.002441\text{ V}$$

$$\%\text{resolution} = \frac{1}{2^{12} - 1} \cdot 100\%$$

$$\%\text{resolution} = 0.0244\%$$

Difference between analog value and digital reconstruction is quantizing error



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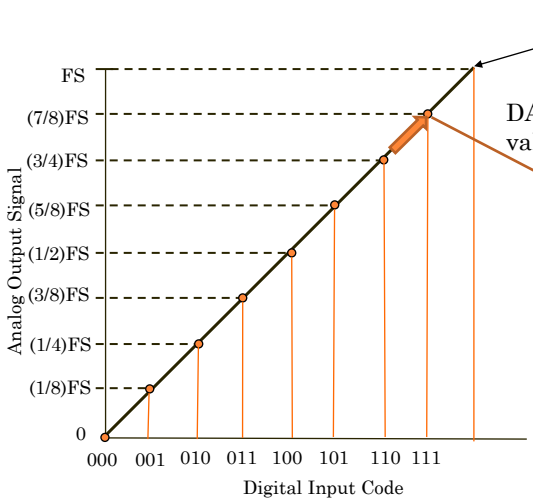
Digital-to-Analog Conversion

Digital-to-Analog Converter (DAC) Transfer Function



DAC produces discrete voltage values for each digital code

Maximum Voltage Output, V_{omax}

$$\text{resolution} = V_{LSB} = \frac{V_{omax}}{2^{n-1}}$$

Max output approaches FS as n goes to infinity

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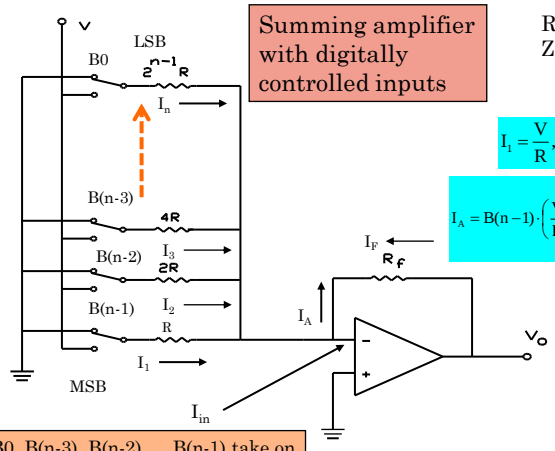
TYPE OF DIGITAL-TO-ANALOG CONVERTERS

Binary-Weighted Resistor DAC



Summing amplifier with digitally controlled inputs

Rules of Ideal OP AMPs $I_{in} = 0$, Z_{in} = infinity

$$I_A = I_1 + I_2 + I_3 .... + I_n$$

$$I_1 = \frac{V}{R},\ I_2 = \frac{V}{2R},\ I_3 = \frac{V}{4R}, ...\ I_n = \frac{V}{(2^{n-1})R}$$

$$I_A = B(n-1)\cdot\left(\frac{V}{R}\right) + B(n-2)\cdot\left(\frac{V}{2R}\right) + B(n-3)\cdot\left(\frac{V}{4R}\right) ... + B0\cdot\left(\frac{V}{(2^{n-1})R}\right)$$

Formula for output V

$$V_0 = -I_F \cdot R_F$$

$$V_0 = -R_F \sum_{i=1}^{n} \frac{B(n-i)\cdot V}{2^{i-1}R}$$

B0, B(n-3), B(n-2), ...B(n-1) take on values of 1 or 0 depending of the digital output controlling switch

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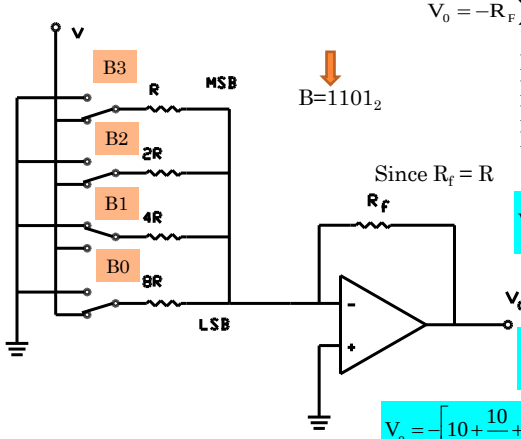
Binary Weighted DAC Example

Example: For the binary-weighted resistor DAC below find the output when the input word is 1101_2 V = 10 Vdc, $R_f = R$

$$V_0 = -R_F \sum_{i=1}^{n} \frac{B(n-i)\cdot V}{2^{i-1}R} \qquad n=4$$



$B=1101_2$

B(4-1)=B3=1 MSB
B(4-2)=B2=1
B(4-3)=B1=0
B(4-4)=B0=1 LSB

Since $R_f = R$

$$V_o = -R\cdot\left[\frac{B3\cdot V}{2^{1-1}R}+\frac{B2\cdot V}{2^{2-1}R}+\frac{B1\cdot V}{2^{3-1}R}+\frac{B0\cdot V}{2^{4-1}R}\right]$$

$$V_o = -\frac{R}{R}\cdot\left[\frac{1\cdot V}{2^0}+\frac{1\cdot V}{2^1}+\frac{0\cdot V}{2^2}+\frac{1\cdot V}{2^3}\right]$$

$$V_o = -1\cdot\left[\frac{1\cdot 10}{2^0}+\frac{1\cdot 10}{2^1}+\frac{0\cdot 10}{2^2}+\frac{1\cdot 10}{2^3}\right]$$

$$V_o = -\left[10+\frac{10}{2}+0+\frac{10}{8}\right] = -[10+5+1.25] = -16.25$$

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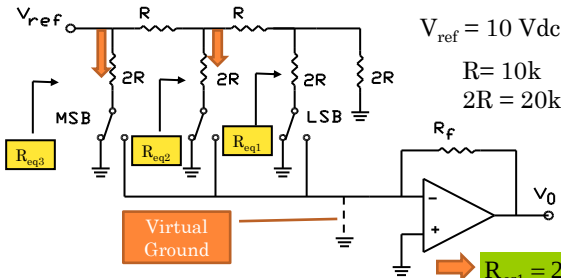
R-2R Binary Ladder DAC

R-2R Ladder produces binary weighted current values from only 2 resistance values.



V_{ref} = 10 Vdc

R= 10k
2R = 20k

Find R_{eq3} by assuming all switches are closed to ground

$$R_{eq1} = 20\,k\Omega \parallel 20\,k\Omega + 10\,k\Omega = 20\,k\Omega$$
$$R_{eq2} = R_{eq1} \parallel 20\,k\Omega + 10\,k\Omega = 20\,k\Omega$$
$$R_{eq3} = R_{eq2} \parallel 20\,k\Omega = 10\,k\Omega$$
$$R_{eq3} = 10\,k\Omega$$

Network equivalent resistance is R

Circuit Analysis

Currents through each 2R value resistor directed to OP AMP or ground by digital switch

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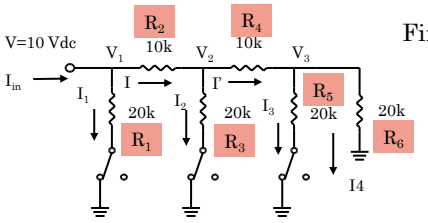
R-2R Ladder Analysis (Continued)



Find I_{in} from R_{eq3} and V

$$I_{in} = \frac{V}{R_{eq3}} = \frac{10\text{ V}}{10\text{ k}\Omega} = 1.0\text{ mA}$$

$$I_1 = \frac{V_1}{R_1} = \frac{10\text{ V}}{20\text{ k}\Omega} = 0.5\text{ mA} \quad I = I_{in} - I_1 = 1\text{ mA} - 0.5\text{ mA} = 0.5\text{ mA}$$

$$V_2 = V_1 - I \cdot R_2 \Rightarrow V_2 = 10 - 0.5\text{ mA} \cdot 10\text{ k}\Omega = 10 - 5 = 5\text{ V}$$

$$I_2 = \frac{V_2}{R_3} = \frac{5\text{ V}}{20\text{ k}\Omega} = 0.25\text{ mA} \quad I' = I_1 - I_2 = 0.5\text{ mA} - 0.25\text{ mA} = 0.25\text{ mA}$$

$$V_3 = V_2 - I' \cdot R_4 \Rightarrow V_3 = 5 - 0.25\text{ mA} \cdot 10\text{ k}\Omega = 5 - 2.5 = 2.5\text{ V}$$

$$I_3 = \frac{V_3}{R_5} = \frac{2.5\text{ V}}{20\text{ k}\Omega} = 0.125\text{ mA} \quad I_4 = \frac{V_3}{R_6} = \frac{2.5\text{ V}}{20\text{ k}\Omega} = 0.125\text{ mA}$$

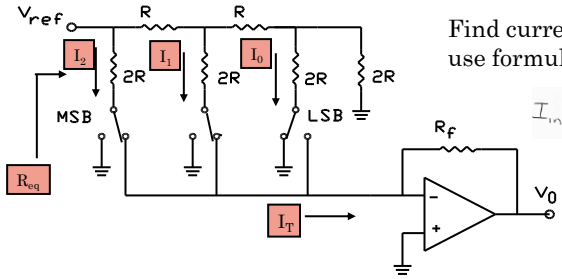
Current Values
I_1 = 0.5 mA MSB
I_2 = 0.25 mA
I_3 = 0.125 mA LSB

Current values directed to OP AMP summing junction or ground. At summing junction:

$$V_o = -R_f \cdot I_T$$

R-2R Example

Find the output voltage for the R-2R DAC shown below. The digital input is 110_2. R=15k, 2R=30k and R_f=15k , Vref=5 Vdc



Find currents I_0, I_1, I_2 and use formula $V_0 = -I_T R_f$

$$I_{in} = \frac{V_{ref}}{R} = \frac{5V}{15k\Omega} = 0.333\text{ mA}$$

$$I_2 = \frac{V_{ref}}{2R} = \frac{5}{30k\Omega} = 0.1667\text{ mA}$$

All other currents reduced by factor of 2.

$$I_1 = \frac{I_2}{2} \Rightarrow I_1 = \frac{0.1667\text{mA}}{2} = 0.0833\text{ mA} = 83.33\,\mu\text{A}$$

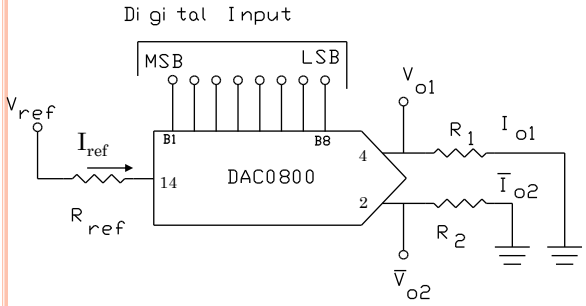
$$I_0 = \frac{I_1}{2} = \frac{0.0833\text{ mA}}{2} = 0.04166\text{ mA} = 41.66\,\mu\text{A}$$

$$I_T = I_2 + I_1 = 0.1667\text{mA} + 0.0833\text{ mA} = 0.25003\text{ mA}$$

$$V_0 = -I_T R_f = -(0.25003\text{ mA})(15\text{ k}\Omega) = -3.75045\text{ V}$$

COMMERCIAL DACS: DAC0800 FAMILY

Devices used in practical designs use integrated R-2R networks and transistor switching. They have TTL compatible inputs.



Design Equations

$$I_{ref} = \frac{V_{ref}}{R_{ref}}$$

$$I_0 = I_{ref}\left(\frac{D}{256}\right)$$

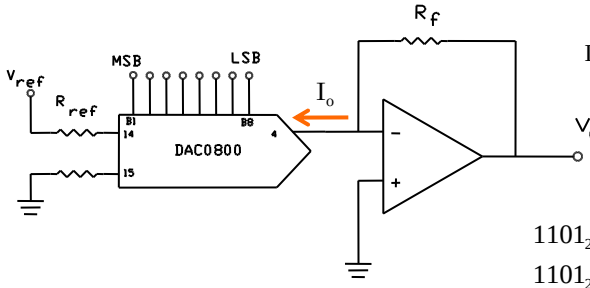
D = decimal equivalent of binary input

8-bit binary code converted to 256 levels of I_0. Full scale value set by reference current. 1 bit change produces change of 1/256 in I_0

$$I_{fs} = \frac{V_{ref}}{R_{ref}}\left(\frac{255}{256}\right)$$ Full scale output

DAC0800 EXAMPLE

Use OP AMP to convert current to voltage. The reference voltage is +10 V dc and the reference resistance is 5kΩ. The value of $R_f = 2.5k\Omega$



$$I_{ref} = \frac{V_{ref}}{R_{ref}} = \frac{10\text{ V}}{5\text{ k}\Omega} = 2.0\text{ mA}$$

a.) convert binary to decimal

$$1101_2 = 2^3(1) + 2^2(1) + 2^1(0) + 2^0(1)$$

$$1101_2 = 8 + 4 + 1 = 13$$

$$D = 13$$

a.) Digital input 00001101_2

b.) Digital input 10001101_2

Find I_0 $\quad I_0 = I_{ref}\left(\frac{D}{256}\right)$

$$I_0 = (2.0\text{ mA})\left[\frac{13}{256}\right] = 0.1015625\text{ mA} = 101.5625\,\mu\text{A}$$

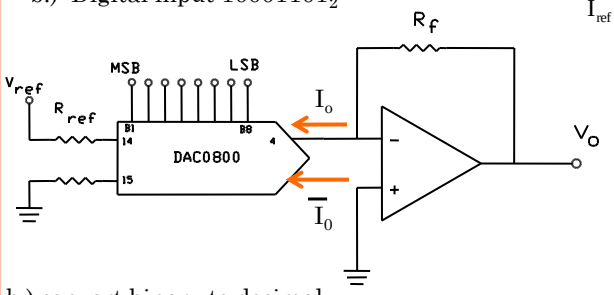
I_o enters so negative

$$V_0 = -(-I_0)\cdot R_f = -(-0.1015625\text{ mA})(2.5\text{ k}\Omega) = 0.253906\text{ V}$$

DAC0800 Example (Continued)

b.) Digital input 10001101_2

$$I_{ref} = \frac{V_{ref}}{R_{ref}} = \frac{10\text{ V}}{5\text{ k}\Omega} = 2.0\text{ mA}$$



b.) convert binary to decimal

$$10001101_2 = 2^7(1)+2^6(0)+2^5(0)+2^4(0)+2^3(1)+2^2(1)+2^1(0)+2^0(1)$$

$$1101_2 = 128+8+4+1 = 141$$

$$D = 141$$

$$I_0 = I_{ref}\left(\frac{D}{256}\right) = (2.0)\cdot\left(\frac{141}{256}\right) = 1.1015626\text{ mA}$$

I_o enters so negative

$$\bar{I}_0 = I_{ref} - I_0 = 2.0 - 1.1015625\text{ mA} = 0.8984375\text{ mA}$$

$$V_0 = -(-I_0)\cdot R_f = -(-1.1015625\text{ mA})(2.5\text{ k}\Omega) = 2.753906\text{ V}$$

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Analog-to-Digital Conversion (ADC)

Converting continuous signals to digital values requires 3 steps

1. Sample analog signal. Nyquist rate or above
   Need a minimum of 2x highest frequency
   Higher rates ease signal reconstruction
2. Hold analog sample while conversion is in progress
3. Convert analog value to digital value (binary)

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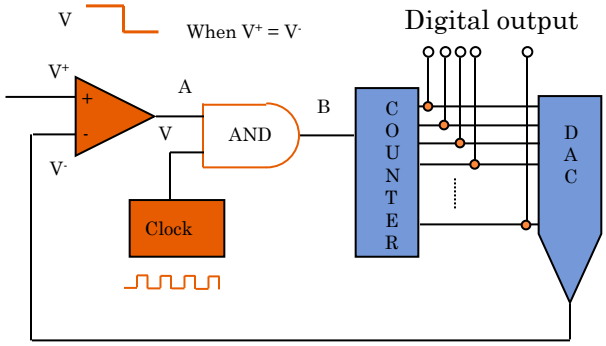
Types of Analog-to-digital Converters

Integrating	Tracking (Counter Type)	Successive Approximation
• High Accuracy • Low Speed • Low Cost • Not commonly used in DAQ	• High Speed in tracking mode • Slow Conversion times (Some Sub-types) • Noise Sensitive	• Conversion time independent of input value • Most commonly used in DAQ applications

Types of Analog-to-digital Converters

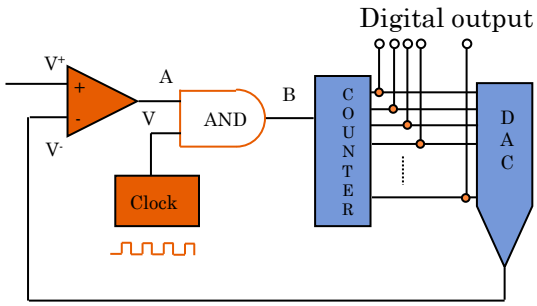
"Flash" or Parallel	Delta/Sigma
• Multi-Comparators • Highest Speed • High Cost	• One bit Conversion • High Resolution • Ratio of 1-to-0 represent input • Uses digital filtering

Counter-Type Analog-to-Digital Converter Operation



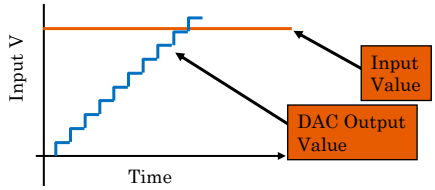
1.) Input a constant value. Requires a sample and hold circuit. (Not Shown)
2.) AND gate passes clock signal when point A logic high
3.) Counter incremented by signal B
4.) DAC output increases as counter output increases

Counter-Type Analog-to-Digital Converter Operation



Tracking A/D converters use up/down counters to minimize conversion times

5.) Counter stops when DAC V exceeds input V



Conversion time depends on the input level

Successive Approximation ADC

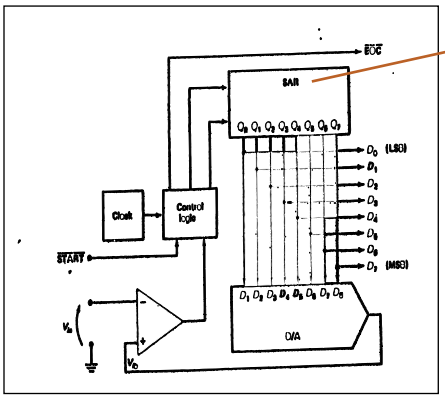
Counter A/D converters conversion time proportional to the input level. Improve conversion speed using a binary search technique.

Procedure

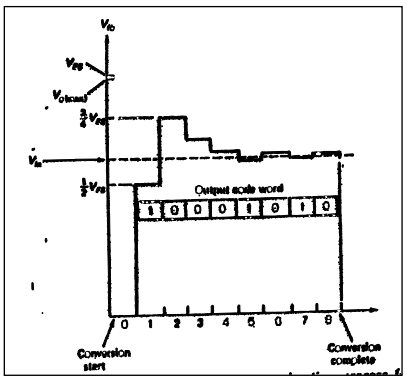
1. Set MSB to 1
2. Test input, V_{in}, against DAC output, V_{DAC}
3. If $V_{DAC} > V_{in}$, reset bit to 0, else bit = 1 ($V_{DAC} < V_{in}$)
4. Move to next bit and repeat steps 1 - 3

The input is converted to digital value in n steps, where n = the number of bits in digital representation

Successive Approximation ADCs



Successive Approx. Register



Successive Approximation ADC

Example: An 8-bit successive approximation ADC has an input voltage of 13.478 V. The ADC full scale input voltage is 20 V. Use the successive approximation algorithm given previously to determine the binary value. Assuming that each bit test takes a single clock cycle, determine the maximum conversion time for the ADC if it is clocked at 4.77 MHz.

Example Solution

Voltage Weight	10.0	5.0	2.5	1.25	0.625	0.3125	0.15625	0.078125	Cycle
Bit	D7	D6	D5	D4	D3	D2	D1	D0	
Set D7	0	0	0	0	0	0	0	0	1
Set D6	1	0	0	0	0	0	0	0	2
Set D5	1	0	0	0	0	0	0	0	3
Set D4	1	0	1	0	0	0	0	0	4
Set D3	1	0	1	0	0	0	0	0	5
Set D2	1	0	1	0	1	0	0	0	6
Set D1	1	0	1	0	1	1	0	0	7
Set D0	1	0	1	0	1	1	0	0	8
	1	1	1	1	1	1	1	1	

1. 10<13.478 bit remains set
2. 10+5>13.478 reset bit
3. 10+2.5<13.478 bit remains set
4. 10+2.5+1.25>13.478 reset bit
5. 10+2.5+0.625<13.478 bit remains set
6. 10+2.5+0.625+0.3125<13.478 bit remains set
7. 10+2.5+0.625+0.3125+.15625>13.478 bit reset
8. 10+2.5+0.625+0.3125+.15625+0.078125>13.478 bit reset

Example Solution (Continued)

Summary Results

Final binary value: $B=10101100_2$

Final voltage: 10+2.5+0.625+0.3125 = 13.4375 V

Quantization Error voltage: V_{QE}=13.478 V-13.4375 V = 0.0405 V or 40.5 mV

Determine conversion time

Define T_c as clock period = $1/f_c$ Where f_c = ADC Clock = 4.77 MHz

$$T_c = \frac{1}{f_c} = \frac{1}{4.77\times10^6\,\text{Hz}} = 2.096\times10^{-7}\,\text{S} = 0.2096\ \mu\text{S}$$

All conversions take 8 clock cycles so maximum conversion time is $8\cdot T_c$

$T_{con} = 8\cdot T_c = 8\cdot(0.2096\ \mu S) =$ **1.667 μS** Ans

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Example Solution (Continued)

What is the highest frequency that the system can convert without folding or aliasing. Assume that the sample and hold time is zero.

Define the maximum conversion rate frequency, $f_{con(max)}$

$$f_{con(max)} = \frac{1}{T_{con}} = \frac{1}{1.677\times10^{-6}\text{S}} = 596{,}250\ \text{Hz}$$

Signals must be sampled at least twice per period (Nyquist rate)

$$2\cdot f_{in} = f_{con(max)}$$

$$f_{in} = \frac{f_{con(max)}}{2} = \frac{596{,}250\ \text{Hz}}{2} = 298{,}125\ \text{Hz}$$ Ans

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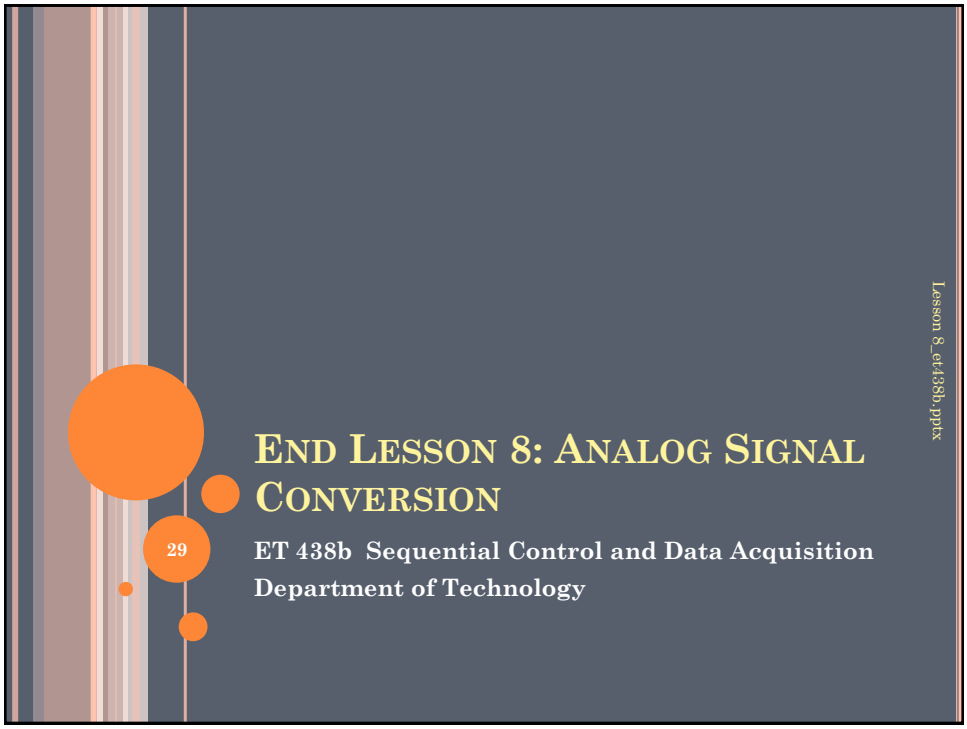
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